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Semiconductor Processing Applied to Integrated Circuit Fabrication

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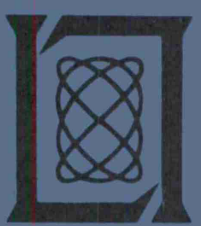

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

SEMICONDUCTOR PROCESSING APPLIED TO INTEGRATED CIRCUIT FABRICATION

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Group 73

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ABSTRACT

This technical note describes the processing steps and technical considerations involved in fabricating bipolar integrated circuits. Basic processes and examples of the use of these to fabricate semiconductor devices are illustrated. A bibliography of basic references to the technology and a short list of current, useful textbooks on the present state of the art are also included.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

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SEMICONDUCTOR PROCESSING
APPLIED TO INTEGRATED CIRCUIT FABRICATION

The semiconductor area in Group 73 is currently under development, and this technical note briefly describes the processing steps and technical considerations involved in fabricating bipolar integrated circuits. The following basic processes are described and comments made on some of the problems associated with each process:

Single-Crystal Material	Photoresist Process
Epitaxial Deposition	Diffusion
Isolation Processes	Metallization
Oxidation	Scribing and Breaking
Mask Making	Die Assembly

The use of these basic processes will be illustrated in the fabrication of a diode, a switching transistor, and an integrated circuit (see Secs. XII-A, -B, and -C, respectively).

I. SINGLE-CRYSTAL MATERIAL

Single-crystal silicon is the material presently used for integrated circuits. An ingot of chemically purified polycrystalline silicon of 5 to 200 ohms-cm p-type is the usual starting material. This crystal is zone refined, i.e., a molten zone is passed slowly through the ingot from one end to the other. The preference for impurities to be in the liquid rather than in the solid zone results in moving the impurities to the end (tail) of the crystal. This tail is removed and the resistivity of the material is checked for intrinsic resistivity. If this resistivity <100 ohms-cm, the material is zone refined again. Special material has been produced up to 1000 ohms-cm. Samples for lifetime measurements are also taken to insure that compensated doping has not produced an "intrinsic" reading.

Single-crystal silicon of desired resistivity[1,2] is prepared from a zone-refined intrinsic polycrystalline ingot, a measured amount of "p"- or "n"-type dopant, and a low imperfection seed crystal with face cut on the desired crystal plane; the ⟨111⟩ plane, which has the greatest density, is the easiest to grow with least chance of polycrystal or twin being formed. A twin is two single crystals growing simultaneously due to (a) imperfections in the boat or seed, (b) mechanical jolting of apparatus, or (c) chemical contamination. The ⟨110⟩ plane is the easiest to scribe and break since its cleavage planes are 90° to each other. The ⟨100⟩ plane gives rise to the lowest number of "surface states" and is used, for example, in MOS devices. The polycrystalline intrinsic material is melted and impurities (dopant) are added. The seed is melted back and a single-crystal silicon of desired orientation, resistivity (Fig. 1), and type is pulled by the Czochralski process (where the seed is dipped into molten silicon and the crystal slowly pulled out), or the float zone process (where the molten zone traverses the seed and ingot in a manner similar to zone refining).

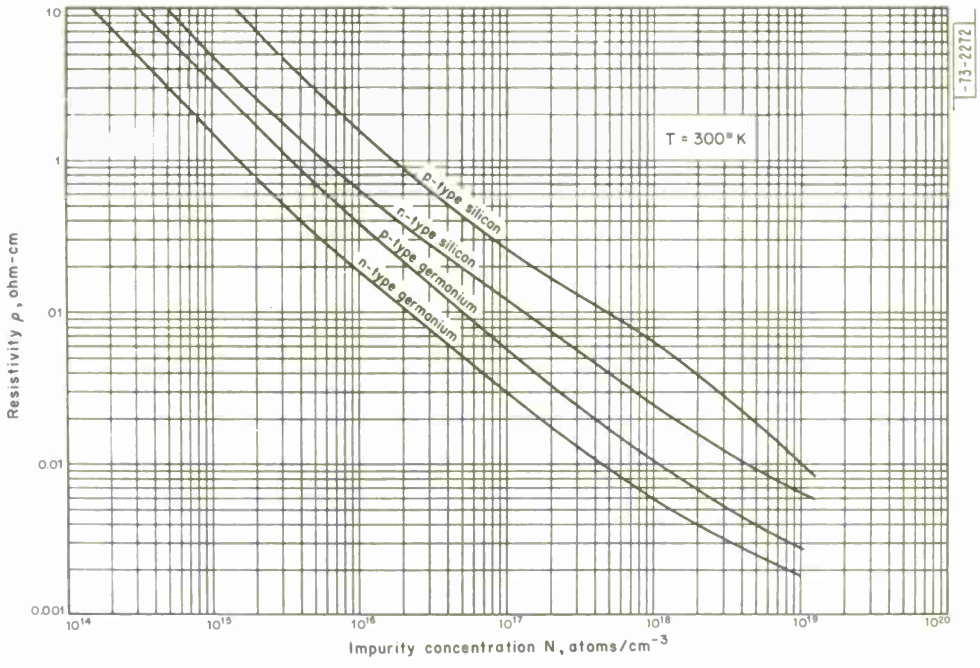


Fig. 1. Resistivity vs impurity concentration.[1,2] [Copyright, 1962, McGraw-Hill, from Transistor Engineering by Alvin B. Phillips; reprinted by permission.]

The float zone material should give more uniform resistivity due to a constant volume liquid zone, while the Czochralski process involves continual depletion of the liquid and also requires a quartz crucible which results in more oxygen being contained in the crystal. An oriented flat is ground on single-crystal ingot (a) to assist in alignment during subsequent processing, and (b) to make scribing and breaking easier by breaking along crystal planes.

The crystal is then sliced with diamond saws into wafer form 10 to 15 mils thick, and the slices are parallel lapped to eliminate saw marks. Finer and finer lapping compounds are used stepwise to reduce surface damage. The final mirror polish is arrived at by either (a) chemical etching which completely removes surface damage but imparts slight unevenness to the surface which can limit subsequent pattern resolution, (b) mechanical polishing which leaves a very flat but slightly damaged surface, or (c) a combination of both. The slice is now ready for buried layer diffusion and epitaxial deposition processes, if required.

II. EPITAXIAL DEPOSITION

The single-crystal silicon substrate establishes the crystal orientation of the epitaxial layer. The usual method is the hydrogen reduction of silicon tetrachloride at approximately 1200°C. The previously lapped and polished wafer is subjected to a final surface treatment in the reactor of anhydrous HCl or H_2O at 1200°C. This removes any remaining surface damage and oxide.

The epitaxial layer is then grown by introducing silicon tetrachloride diluted with H_2 and small amounts of H_2 containing phosphine or diborane. For n- and p-type layers, respectively, a good epitaxial system should be capable of 100-ohm-cm layers. Growth rates vary with time and temperature and are of the order of 1 micron/minute. Cleanliness and reagent purity are most important. Starting materials must be free of imperfections, as this process worsens their

condition. Most layers are in the resistivity range of 0.1 to 10 ohms-cm (Fig. 1) and thickness of 3 to 30 microns. Good control of reagents, gas flow, etc., can result in variations of less than ±10 percent across a wafer. Caution must be taken due to the toxic and explosive nature of gases used.

III. ISOLATION PROCESSES

Some devices in integrated circuits must be electrically isolated from the rest of the circuit. This is accomplished in several ways.

A. Diffusion Isolation[3] (Fig. 2)

Isolation is accomplished by diffusing p-type grid into a thin n epi-layer at high temperatures (1250°C) for a relatively long time (2 to 4 hours) until it reaches the p-type substrate.

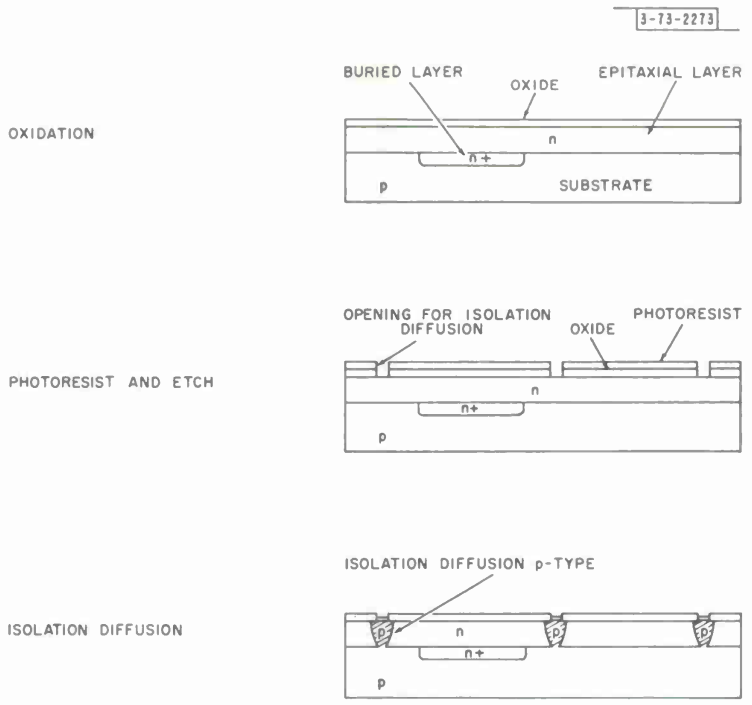


Fig. 2. Diffusion isolation.

B. Dielectric Isolation[4] (Fig. 3)

(1) n on n+ (by buried or epitaxial layer) substrate is oxidized.

(2) The oxide is etched except where isolated islands of silicon are required.

(3) The silicon substrate is etched to form a moat around the islands.

(4) The silicon is reoxidized.

(5) Polycrystalline silicon is deposited to a thickness of several mils.

(6) The original n-layer is lapped down to the oxide-coated moat and reoxidized.

(7) The wafer is inverted and we now have a polycrystalline silicon slice with thin n on n+ islands isolated by SiO_2 tubs. A similar method[5] does not require lapping the device area.

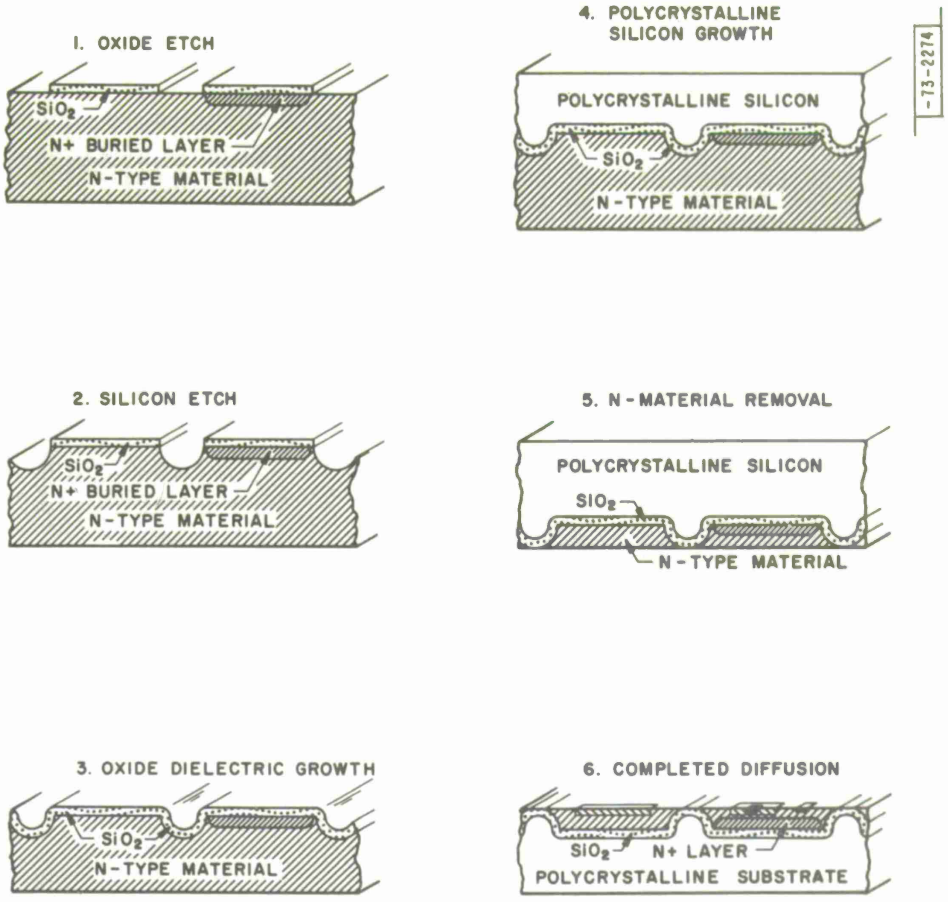


Fig. 3. Dielectric isolation. [Copyright, 1966, Integrated Circuit Engineering Corporation, Phoenix, Arizona, from Integrated Circuit Engineering, 4th Edition (Boston Technical Publishers, Inc., Cambridge, Massachusetts); reprinted by permission.]

C. Air Gap Isolation – Beam Leads[6] (Fig. 4)

(1) The wafer is prepared in the normal fashion up to the metallization step.

(2) Platinum is sputtered and alloyed into the contact windows. The platinum silicide that is formed gives good ohmic contact. The unreacted platinum is removed by back sputtering.

(3) The oxide is etched, leaving an overhang to prevent shorts from the beams to the substrate.

(4) Titanium/platinum is sputtered and gold evaporated for conductor paths. By photoresist masking, gold is plated up to 0.3 to 0.5 mil. The photoresist is removed and titanium/platinum are removed by back sputtering. Conductor paths remain where the gold was plated.

(5) Finally, the slice is thinned down to approximately 1 to 2 mils.

(6) Isolation paths are lined up for both the front and back of the wafer with a backside or infrared aligner. The silicon is etched away leaving desired areas isolated by air, each isolated area held together with gold beams. Some beams are allowed to overhang the die for external connections.

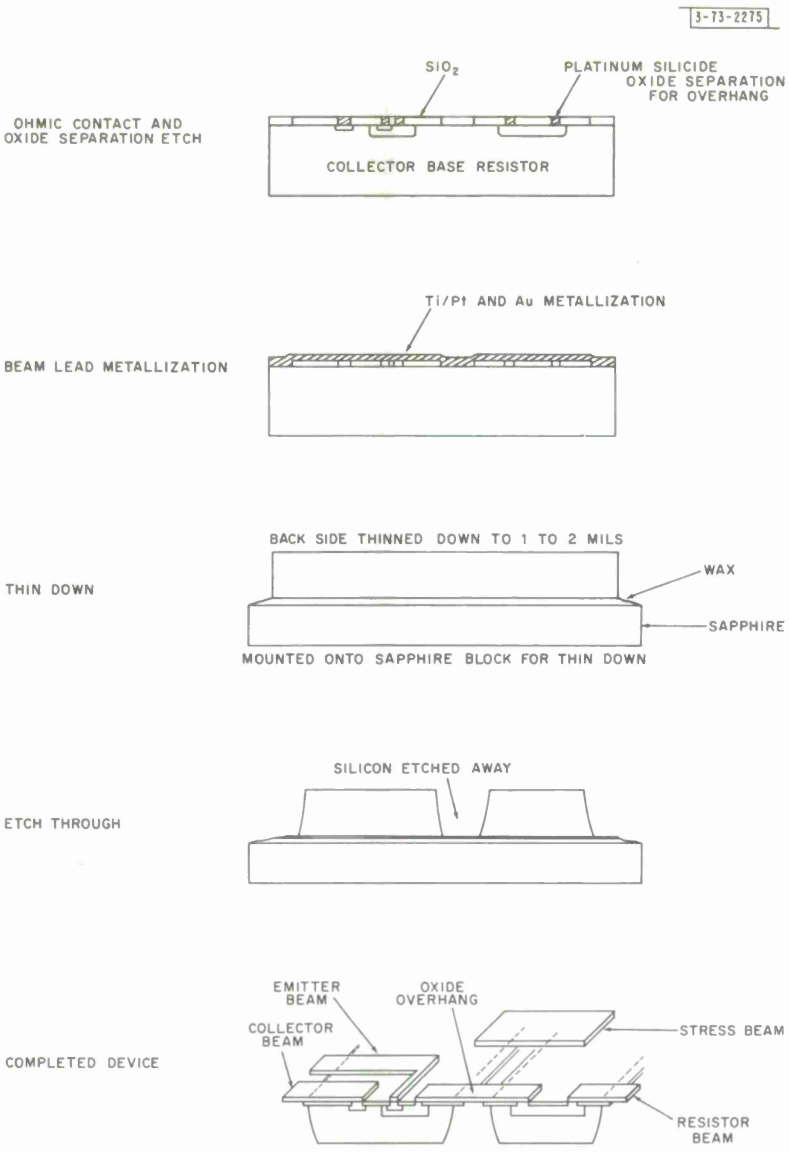


Fig. 4. Air gap isolation (beam lead).

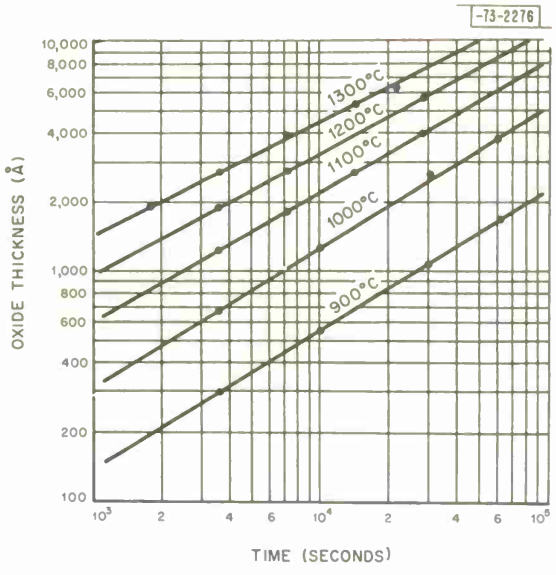


Fig. 5. Oxidation of silicon in dry oxygen.[7] [Copyright, 1965, McGraw-Hill; reprinted by permission.*]

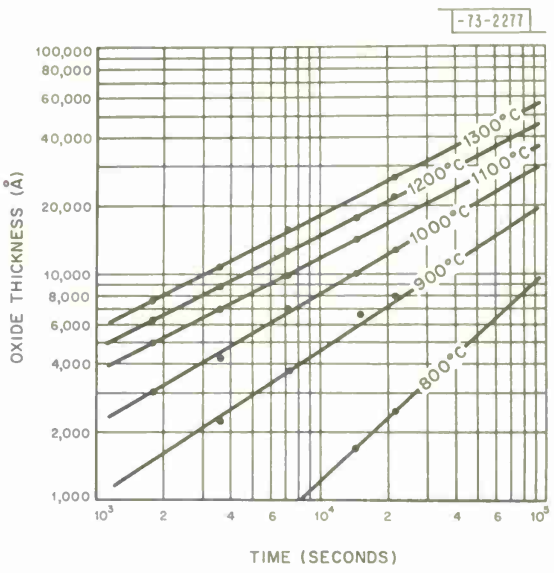


Fig. 6. Oxidation of silicon in steam.[7] [Copyright, 1965, McGraw-Hill; reprinted by permission.*]

IV. OXIDATION

The planar process owes its existence to the fact that silicon dioxide exhibits the following properties:

(a) The oxide mask is an effective mask against boron and phosphorus.

(b) The oxide passivates the surface of silicon protecting the junction.

(c) The oxide is a good dielectric.

(d) The oxide may be etched with good resolution.

(e) The oxide forms a uniform, controlled thickness on the silicon with similar thermal expansion properties.

Oxidation is performed in an open-tube furnace at 900° to 1250°C by passing pure oxygen gas in a dry or wet[7] state over the silicon surface. Layers from a few hundred to several thousand angstroms can be grown in a reasonable amount of time, although dry oxygen is considerably slower than wet oxygen (Figs. 5 and 6). About 40 percent of the oxide layer is below the original silicon surface. The dry oxide is particularly useful for high-voltage and MOS devices due to its low surface state density. Dopants can diffuse laterally under SiO_2 (approximately 83 percent of the diffusion depth), resulting in the p-n junction being under a passivated surface.

V. MASK MAKING

The design and layout of masks are necessary for each major step. Each mask has a specific function in the fabrication of an integrated circuit. An example of masking follows for the p-type integrated circuit substrate.

Mask 1. Buried Layer:— Used to define an n+ region for the reduction of collector series resistance, and applied prior to the epitaxial deposition.

Mask 2. Isolation Diffusion:— Defines separate n-type islands in the epitaxial layer. The islands are isolated by reverse-bias p-n junction.

* From Integrated Circuits, Raymond M. Warner, Jr., Editor.

Mask 3. Base Diffusion:— Defines a base region of a transistor and the area for the diodes, resistors, and capacitors.

Mask 4. Emitter Diffusion:— Defines an emitter region for transistors, crossovers, and n+ collector contact areas.

Mask 5. Contact:— Defines metallization areas for ohmic contact.

Mask 6. Metallization:— Defines interconnecting conductor pattern, bonding pads, and ohmic contacts to circuit elements.

Patterns are drawn to large scale and reproduced by cutting rubylith material which is then photographically reduced twice; the second reduction is by a step-and-repeat process to form a master mask. At this point, desired copies are printed. Another method employs a fly's eye camera which performs reduction and repeating concurrently. However, resolution tends to fall off near the edge of the pattern. Computer programming is also presently being employed to provide a paper tape to operate a pattern generator which produces a finished mask. Masks are usually made of an emulsion on glass which is subject to scratching and tearing when in contact with wafers and must be regularly replaced. Also available are chromium masks which are more expensive but last much longer in production. Resolution is claimed to be better since the thickness of the chromium layer is less than that of the emulsion. Considerable research is being done on the utilization of electron-beam technology to make masks and also to expose photoresist patterns directly without use of masks. Resolution of 0.1 micron is possible with electron-beam processing.

VI. PHOTORESIST PROCESS[8]

The oxide-coated wafer is placed on the vacuum chuck of the photoresist spinner. The photoresist, usually diluted and filtered, is dropped on the wafer providing a complete coating. Excess photoresist film is thrown off by spinning the wafer at several thousand rpm for 5 to 30 sec. Coating thickness is determined by the rise time of the motor, spinning speed, time of spinning, and viscosity of photoresist which is affected by temperature and dilution. The coating is dried at approximately 100°C for one-half hour to remove solvents. The appropriate pattern is now printed on the wafer by aligning the coated wafer with appropriate masks in an alignment machine equipped with high-power split-field optics, accurate micrometer stage (1 micron or less) with X, Y, and Θ controls, and collimated ultraviolet light source. After alignment is made, the wafer is lifted into direct contact with the mask and exposed to ultraviolet light. Then, the wafer is removed and the unexposed resist developed out with an appropriate solvent. The wafer is now baked at a higher temperature (180°C) so that it will resist the etching process. A buffered HF solution is used to etch windows in the exposed SiO_2. After etching, the remaining acid is rinsed away and the resist is removed by a hot fuming sulfuric acid bath or by commercial resist removers, such as J-100. The wafer is then rinsed in running distilled deionized water, dried, and made ready for the next diffusion cycle. Note that the adhesion of the resist is affected by many variables, such as humidity, composition of the oxide, surface treatment of the wafer before the application of the resist, time in the acid, composition of the acid, focusing of ultraviolet light, distance between the mask and the wafer during exposure, and thickness of the resist and emulsion. Resolution is principally determined by the resolution of the mask, nature and thickness of the resist, mask emulsion and oxide, and flatness of the wafer.

VII. DIFFUSION

Diffusion[9] is a process of incorporating impurity atoms (dopant) into single-crystal silicon. By controlling conditions carefully, one can obtain various surface concentrations, depths, and profiles of p-n junctions. This profile depends upon the following:

(a) Level and distribution of dopant.

(b) Time and temperature of deposition and diffusion.

(c) Diffusion coefficient, solid solubility, and other characteristics of the dopants.

(d) Amount and form of dopant.

There are two general types of diffusion profiles.

(a) Error function (Fig. 7). Here, the unlimited dopant source is continually diffused into the semiconductor, and the surface concentration approaches the maximum solid solubility. It is used where high surface concentration is required, such as emitters and contacts. This profile can be approximated mathematically as

$$N(x, t) = No \operatorname{erfc} \frac{x}{\sqrt{4Dt}}$$

where

N = impurity atom concentration at the junction,

No = impurity atom concentration at the surface,

x = junction depth (cm),

D = diffusion coefficient (cm^2/sec),

t = diffusion time (sec).

(b) Gaussian (Fig. 8). Here, a short low-temperature diffusion (called deposition) is performed on the semiconductor. The dopant source is removed and the diffusion is carried out at a higher temperature, redistributing the available dopant. It is used where low surface concentration (base regions) and high-resistivity layers (resistors) are desired. This profile can be approximated mathematically as

$$N(x, t) = Noe \frac{-x^2}{4Dt}$$

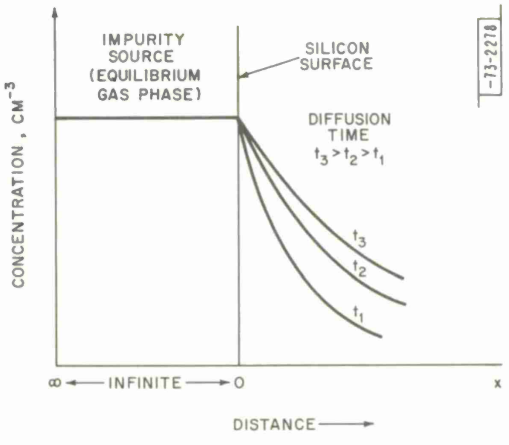


Fig. 7. Complementary error function diffusion profile. [Copyright, 1965, McGraw-Hill; reprinted by permission.*]

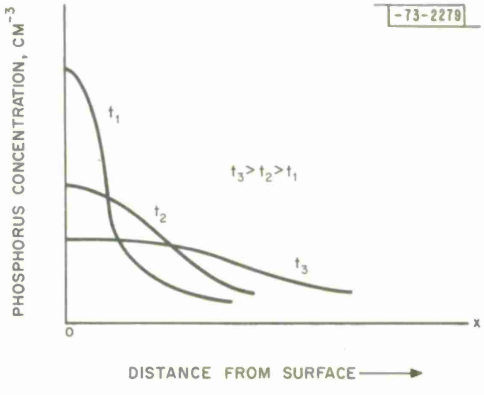


Fig. 8. Gaussian diffusion profile. [Copyright, 1965, McGraw-Hill; reprinted by permission.*]

* From Integrated Circuits, Raymond M. Warner, Jr., Editor.

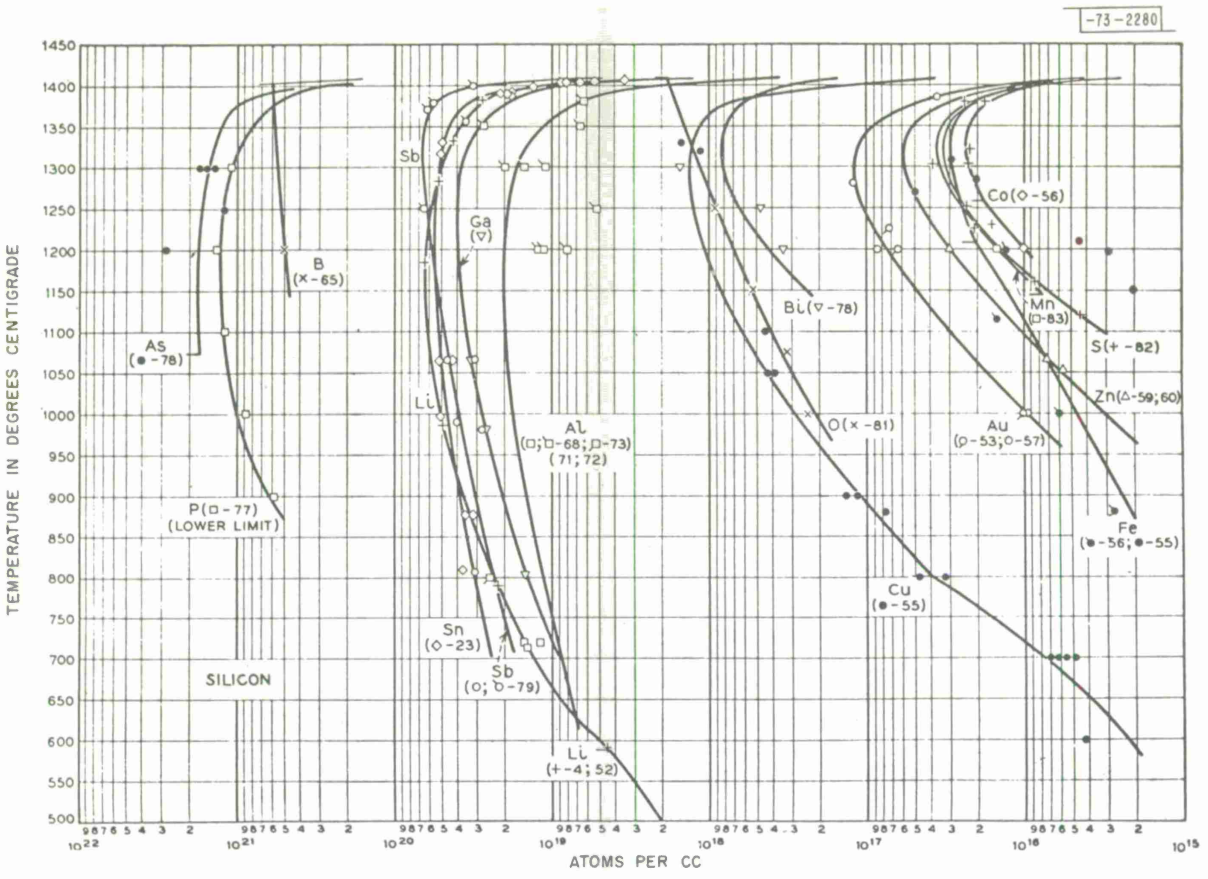


Fig. 9. Solid solubility of impurity elements in silicon.[10] [Copyright, 1960, The American Telephone and Telegraph Co., reprinted by permission.]

Each dopant material has individual characteristics, such as type (p or n) solid solubility[10] (Fig. 9) (maximum surface concentration), and diffusion coefficient[11] (Fig. 10) (rate of diffusion vs temperature). Special characteristics are noted also; for example – phosphorus is affected easily by moisture, and gold is a very fast diffuser and lowers the lifetime of silicon significantly.

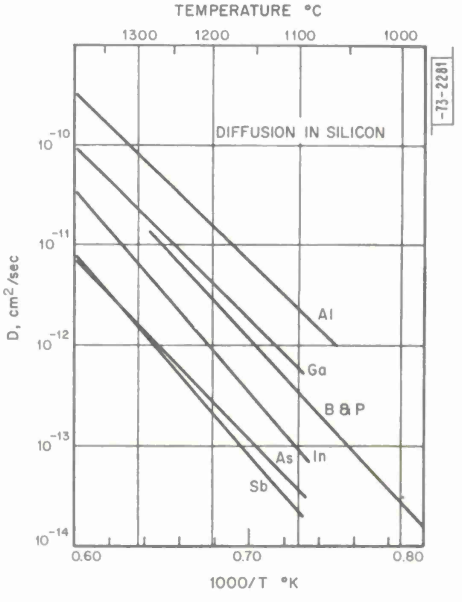
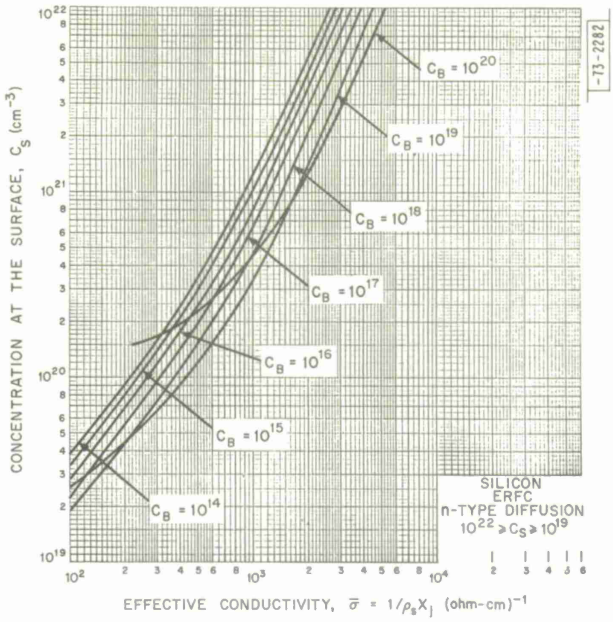
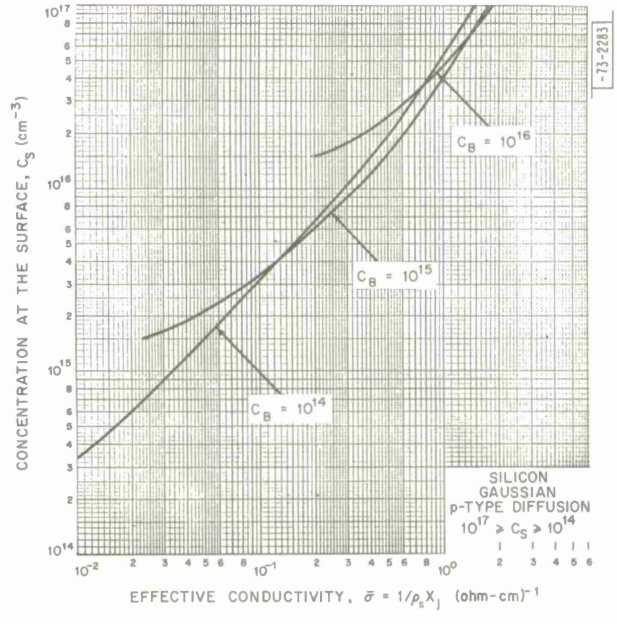


Fig. 10. Diffusion coefficients of impurities in silicon.[11] [Copyright, 1962, McGraw-Hill, from Transistor Engineering by Alvin B. Phillips; reprinted by permission.]



(a)



(b)

Fig. 11(a-b). Effective conductivity of diffused layers.[12] [Copyright, 1962, The American Telephone and Telegraph Co., reprinted by permission.]

Diffusion processing is considered "black magic" in many ways. Several entirely different systems can give identical electrical results; contrastingly, several seemingly similar systems can give different results. Although there are many diffusion systems, the one overwhelmingly used is the open-tube process. Here, the source (dopant) as a gas, liquid, or solid at room temperature or elevated temperature is flowed over the silicon wafer at 900° to 1250°C by a carrier gas, usually N_2 and/or O_2. Time, temperature, complementary error function or Gaussian conditions, and oxidizing or nonoxidizing ambient conditions determine the surface concentration, junction depth, and profile or gradient of the resulting diffusion. The effect of diffusing into a previously diffused wafer must be taken into consideration when selecting dopant, time, temperature, and other conditions in order to obtain a proper relationship of p-n junctions to each other (base width, concentration gradient). This relationship determines resulting electrical parameters (e.g., Beta, storage time) of semiconductor devices as much as initial device design (geometry of masks). Cleanliness is extremely important here, particularly in equipment, chemicals, wafers, and gas supply. Most of the gases used are toxic and must be handled with care. Several of the more important variables are:

(a) Time and temperature of diffusion (less than ±0.5°C temperature variation over the flat zone length is required).

(b) Control of amount, source, vapor pressure, and purity of dopants. (Dopants must be kept separate and prevented from intermixing with each other.)

(c) Uniform flow of dopant around wafer.

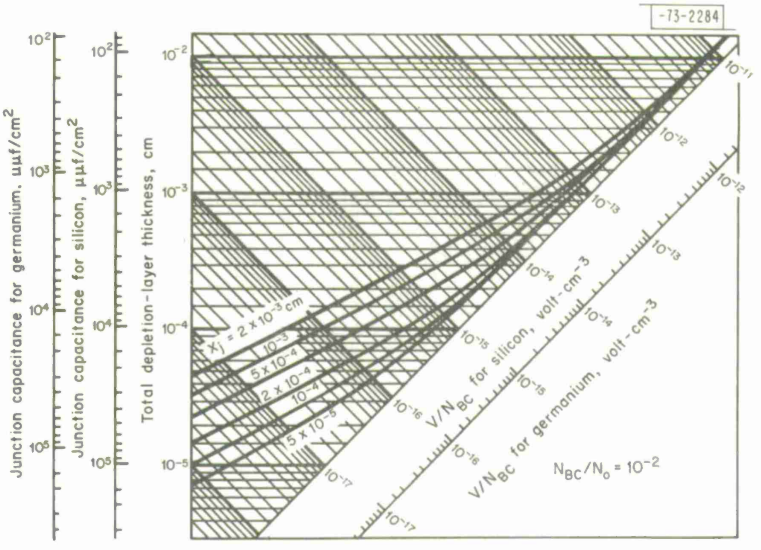
(d) Cleanliness. (Elimination of undesirable secondary sources, and effects.)

Evaluation of the diffusion requires electrical test equipment with a prober, a resistivity kit, bevel and stain facilities, and a microscope to determine surface concentrations, junction depths, and surface conditions. Irvin's curves[12] [Figs. 11(a) and (b)] and those of Lawrence and Warner[13] [Figs. 12(a) and (b)] are used to determine the electrical parameters of diffused layers from the above test data.

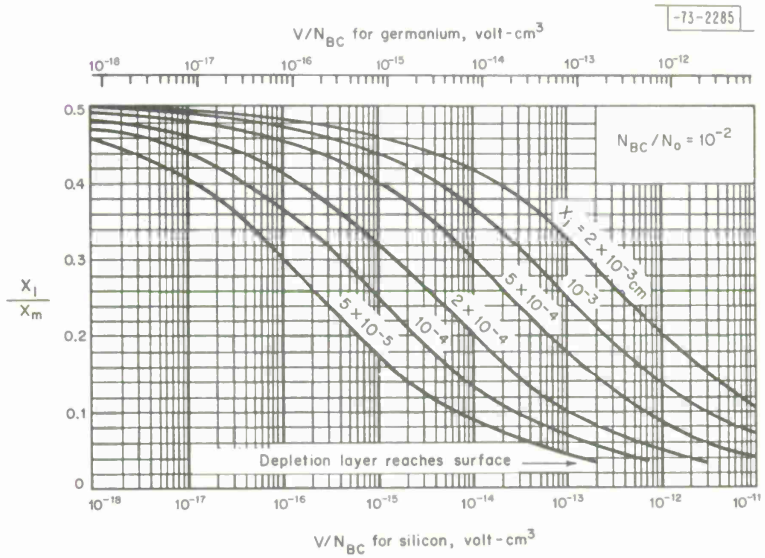
VIII. METALLIZATION

Aluminum (Al) is the most commonly used metallization for integrated circuits because it forms an ohmic contact with p-type and heavily doped n-type silicon, adheres strongly to silicon and silicon dioxide, and is a good conductor. However, if gold (Au) wire is used for bonding, there is a possibility of a brittle Au-Al compound (purple plague) being formed at high temperatures. If Al wire is used, it must be bonded to Au-plated posts where plague is less likely. Au metallization can be used to eliminate this problem. However, Au does not adhere to SiO_2; thus, Cr, Mo, and Ti are used with Au. However, these metals do not make as good an ohmic contact as Al. In the beam lead process, the metallization system is more complex. Platinum is used to form platinum silicide (for ohmic contact) with silicon, titanium for forming bonds to SiO_2, and gold to conduct and serve as a bonding "wire" and to hold isolation regions together. The resulting Au-Au bonded system gives the best bond possible.

Ultra-pure metals are evaporated from tungsten coils in standard oil diffusion pump evaporators in a vacuum of at least 10^{-6} mmHg using a liquid nitrogen cold trap. If further cleanliness is necessary, such as for MOS devices, an oil-free vacuum system incorporating cryogenic



(a)



(b)

Fig. 12(a-b). Graded junction curves.[13] [Copyright, 1962, McGraw-Hill, from Transistor Engineering by Alvin B. Phillips; reprinted by permission.]

absorption pumps and titanium chemical pumps can be used in conjunction with electron beam gun evaporation from a cooled crucible. In either case, equipment and material cleanliness are absolutely necessary here. The usual vacuum technology procedures apply. Some of the variables encountered are:

(a) Cleanliness of the metal substrate, the interior of the vacuum chamber, and the bell jar
(b) Substrate temperature control
(c) Amounts evaporated
(d) Time of evaporation
(e) Shutter variables
(f) Vacuum level employed
(g) Positioning accuracy.

These variables can affect the film's adhesion, thickness and uniformity (shadowing), electrical characteristics (resistance), and may subsequently affect bonding and reliability. The conductor pattern is then made using standard photoresist techniques and applicable etch methods. Sputtering and plating are two other techniques used less frequently for metallization.

To insure proper ohmic contact, the wafer is generally alloyed or sintered at or near the eutectic point for a few moments in an inert or reducing atmosphere. Up to this point, the wafer has been carried through the process at 5 to 8 mils thick to reduce breakage. Here, the wafer is thinned down to approximately 4 mils and a gold evaporation is performed as an aid to eutectic die mounting. All the devices on the wafer are electrically checked at this point, and bad ones are inked out. This is usually an automatic or semiautomatic operation.

IX. SCRIBING AND BREAKING

Utmost care must be taken to scribe, especially in the case of dice <20 mils square. The ratio of edge to thickness is reduced drastically as the die size gets smaller and the yield is reduced. Most slices are made with no oxide on the edge of the cell pattern, leaving a gridwork of bare silicon 2 to 4 mils wide. The diamond scribe point should ride in this area as it is difficult for the scribe point to penetrate the oxide area. Automatic machines are available for this step, but much is left to the operator in determining diamond tip quality, pressure, angle, and tracking. Machines exist for breaking, but, in many cases, the slice is rolled over small-diameter steel rods and is usually mounted in wax or ice to improve breaking characteristics. At present, there is no uniform practice for breaking. Essentially, the larger and thinner the die, the easier it breaks. The devices which are not inked out in prior test are selected, visually inspected, and sent on to final assembly.

X. DIE ASSEMBLY

A. Die Mounting

The principal method used for die attachment is eutectic die bonding; this involves mounting a gold or n- or p-type doped gold-backed die with or without a corresponding preform onto a gold-plated substrate. The combined assembly is heated to slightly above the melting point of the eutectic mixture[14] of Au/Si (Fig. 13), and the die is scrubbed with tweezers or an ultrasonic fixture. The gold dissolves into the silicon until the composition is that of a gold silicon eutectic mixture, whereupon further dissolution causes freezing if the temperature is maintained constant

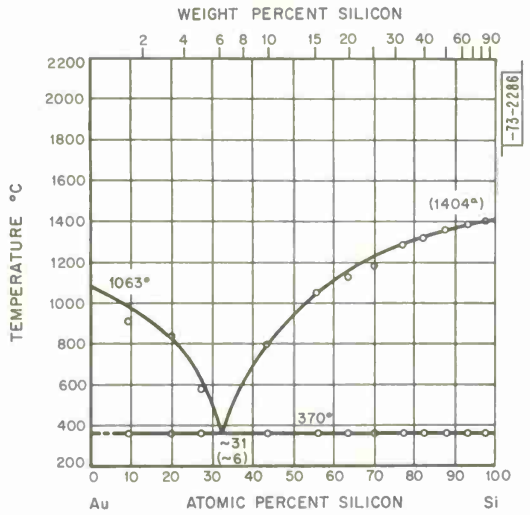


Fig. 13. Gold-silicon phase diagram.[14] [Copyright, 1966, Integrated Circuit Engineering Corporation, Phoenix, Arizona, from Integrated Circuit Engineering, 4th Edition (Boston Technical Publishers, Inc., Cambridge, Massachusetts); reprinted by permission.]

and bonding is effected. The operation is usually performed on special die bonding equipment on a hot stage in an inert atmosphere. By using different composition preforms, varied bonding temperatures can be used.

For especially good ohmic contact, in the case of power transistors for example, the back of the die has a nickel evaporation or plating and a solder preform is used which melts and attaches to nickel but does not form an eutectic mixture. To freeze this, one must cool to below the freezing point of the solder.

B. Wire Bonding

Aluminum or gold wires are most frequently used for semiconductor work. Special equipment capable of handling wire as small as 0.5 mil in diameter is used which can locate the wire on an area as small as 1 square mil. The substrate containing the mounted die is heated in an inert atmosphere and the wire is bonded by one of the following methods.

1. Thermal Compression

a. Wedge Bonding

The wire is positioned on the pad and a heated tungsten carbide wedge tip depresses the wire on the pad. The wire is then moved to a second connecting point and the process is repeated, whereupon the end of the wire is melted off with a capillary H_2 flame. This method, though slow, is still used extensively.

b. Ball Bonding

Gold wire is used in ball bonding since aluminum does not form a usable ball. The ball is formed by a H_2 flame-off tool. The wire is forced onto the pad with a heated capillary tool which also feeds the wire. Then, the wire is moved to a second connection and depressed again and cut off by a H_2 torch forming a new ball. This process is faster and forms a good bond due to the large contact area of the ball, but, of course, it requires large bonding pad areas.

c. Stitch Bonding

Stitch bonding is similar to ball bonding except that no ball is formed. Wire is fed from a heated capillary tool depressed on the pad, then moved to a second connecting point but cut off by a mechanical tool to avoid forming a ball. The process is fast and, when small wires are used, is quite applicable for bonding to small pad areas. Al wire can be stitch bonded.

2. Ultrasonic Bonding

Little or no heat is required in this case, since the ultrasonic tool vibrates the wire and breaks down any oxide interface to form a strong intermolecular bond with Al or Au. This procedure is especially applicable to heat-sensitive dice or where temperatures must not be maintained for a long period of time. It is also used for bonding large-diameter wire, i.e., wire >3 mils.

XI. GENERAL

Cleanliness and ambient control are required at every step in the process. Distilled deionized water is used for all rinsing and cleaning with a minimum of 10 to 12 megohms-cm required, and 18 megohms-cm desired. Process and humidity control is maintained throughout the area with either local dust-free Class 100 ambients maintained for critical operation, or the entire operation is performed in a clean room of acceptable class.

XII. SILICON PLANAR FABRICATION PROCESSES

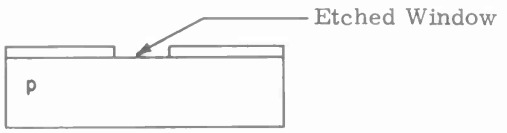
A. Diode

The following sequence of steps will show the fabrication of a silicon planar diode.

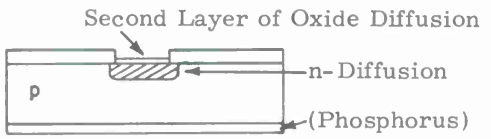
1. Material: In this device, material used is single-crystal silicon slice. Orientation is ⟨111⟩ plane with resistivity of 0.3 to 0.5 ohm-cm p-type.

2. Oxidation: This step will grow 6000 Å of oxide in 1 hour, which will be sufficient oxide to mask the following diffusion.

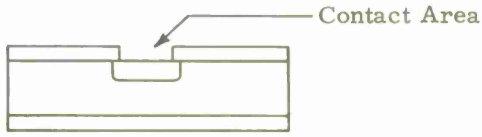
3. Anode Mask: Photoresist process to open the anode window for diffusion; approximately 5 mils diameter.



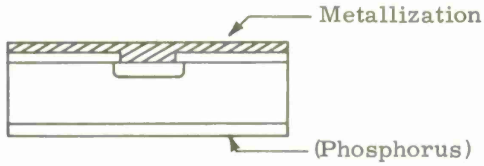
4. n-Diffusion: Complementary error function diffusion of phosphorus impurities into front and back side of slice. Phosphorus on back side helps getter impurities. The Co will be approximately 10^{21} atoms/cc and depth of 2 microns. This will produce high efficiency and good ohmic contact. Depth insures passivated junction and reasonable breakdown voltage. A low-temperature (900°C) oxidation is now made to help protect junction from contamination.



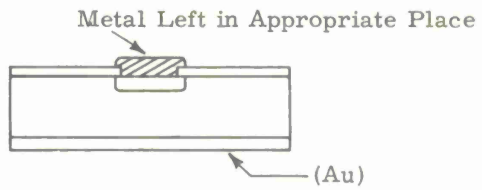
5. Contact Mask: Photoresist process to open window for metallization approximately 4 mils diameter.



6. Metallization: Approximately 5000 Å thick of metal (normally aluminum) is evaporated at 10^{-6} mmHg over entire surface of slice.



7. Metallization Mask: Photoresist process to etch away all unnecessary metal and form contact and bonding areas. Slice is then sintered at approximately 570°C. Back side phosphorus layer is etched off and gold evaporated to insure good mounting.

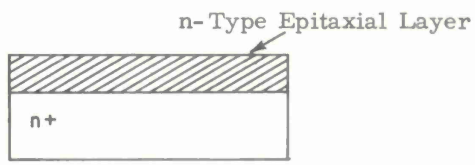


B. Switching Transistor

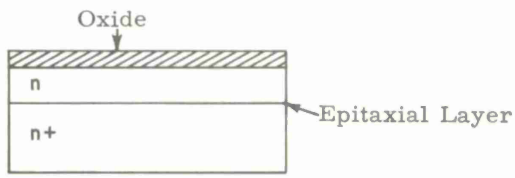
The following steps show the process necessary to fabricate an n-p-n switching bipolar transistor. The general procedure is adaptable to all bipolar transistors.

1. Material: Starting material is slice of 0.005 to 0.009 ohm-cm Sb-doped n-type ⟨111⟩ oriented single-crystal silicon. This low-resistivity material is used because it greatly decreases collector series resistance.

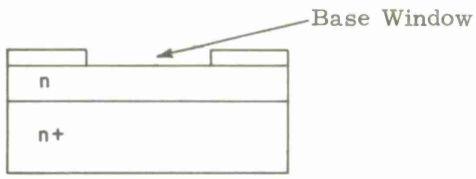
2. Epi-Layer: An n-type epitaxial layer is grown in an RF reactor at approximately 1200°C. Layer is 6 to 10 μ thick with resistivity of 0.1 to 0.3 ohm-cm. Resistivity and thickness of epi-layer must be optimized to provide maximum breakdown voltage and minimum series resistance.



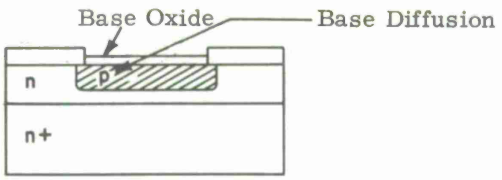
3. Oxidation: First oxidation is grown in 1100°C wet oxygen environment for 1 hour. This will produce 4000 to 6000 Å which will be enough to mask the following diffusion.



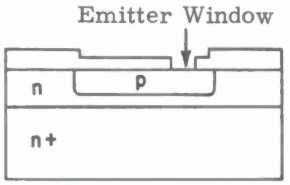
4. Base Mask: Photoresist will be applied to open the window for base diffusion. Window opening is 4 × 5 mils.



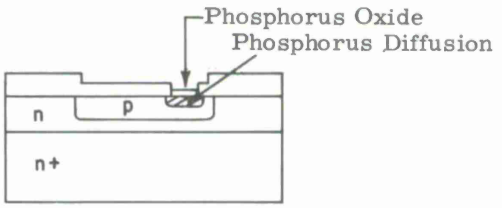
5. Base Diffusion: This p-type boron (BB_{r3}) diffusion will be a Gaussian distribution diffusion and will obtain surface concentration (Co) of 4×10^{19} atoms/cc and depth of 12,000 Å. Deposition will be done at 1100°C for 10 minutes. Slice is then gold evaporated on back side just prior to diffusion to reduce storage time (Ts). From here, slice is put into 1100°C oxidation for 45 minutes where diffusion to depth takes place. This oxide will also passivate junction and mask off emitter diffusion yet to come.



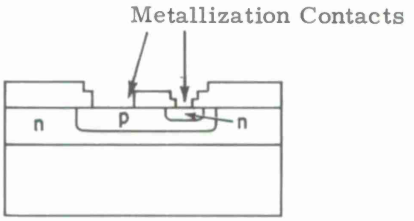
6. Emitter Mask: This photoresist will be to open a window in base region for emitter diffusion (1 × 3 mils).



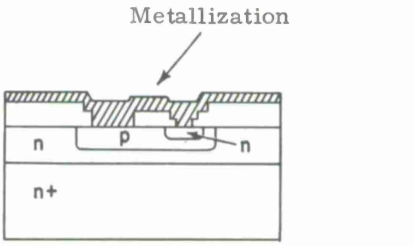
7. Emitter Diffusion: Here, an n-type ($POCl_3$) dopant is diffused into the emitter window. Diffusion is essentially an error function diffusion 9500 Å deep with Co of 10^{21} atoms/cc. Base width will be 2500 Å which is necessary to obtain electrical parameters required for this device. (Beta, transit time, BVCEO.)



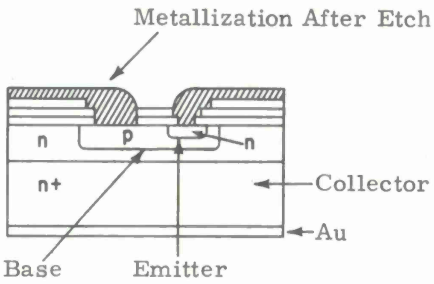
8. Contact Mask: Another mask is now applied which will open base and emitter contact areas (0.8 × 2.5 mils) for metallization. It is important here that all oxide be removed prior to metallization. Any oxide will hinder good ohmic contact.



9. Metallization: Aluminum metal (5000 Å) is now evaporated over entire surface of slice.



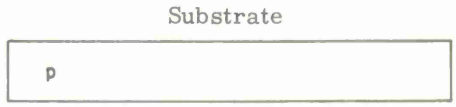
10. Metallization Mask: Final photoresist process is carried out on the metal which is then etched leaving metal for contact and bonding areas. Aluminum is sintered at 570°C, back side is etched and gold evaporated to insure good mounting.



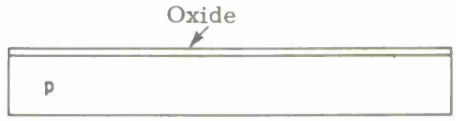
C. Integrated Circuit

The following steps will show the fabrication of a simplified circuit employing a transistor and resistor. This circuit can be expanded readily by adding capacitors, diodes, and resistors, if desired.

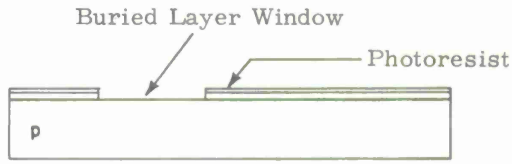
1. Material: A p-type (boron) slice 6 to 7 mils thick, 7 to 14 ohms-cm. High-resistivity material limits back diffusion into epitaxial layer.



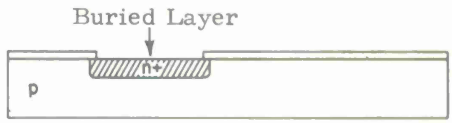
2. Oxidation: A 6000-Å oxide is grown to mask off buried layer diffusion.



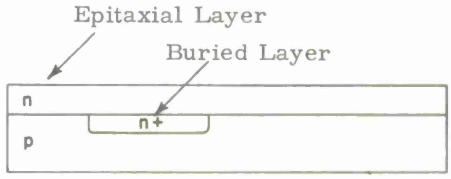
3. Buried Layer Mask: To open window in oxide to protect against diffusion.



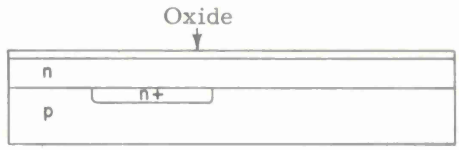
4. Buried Layer: High-concentration complementary error function, Co = 10^{21} atoms/cc n-type (Sb) diffused in 3 microns. This diffusion is made to decrease collector series resistance.



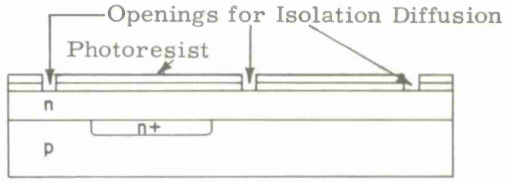
5. Epitaxial Layer: A thin 6- to 20-micron n-type (phosphorus) epitaxial layer is grown in a reactor. This layer is collector area for transistors.



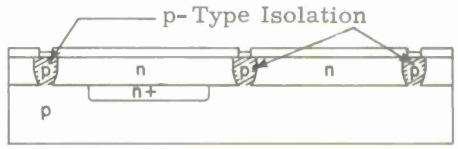
6. Second Oxide: 10,000 Å protecting epitaxial layer from deep isolation diffusion.



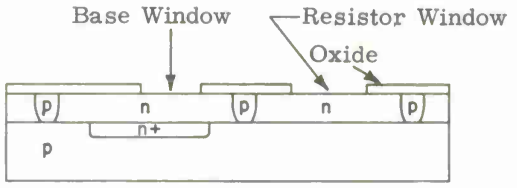
7. Isolation Mask: Opening of areas in oxide for isolation diffusion.



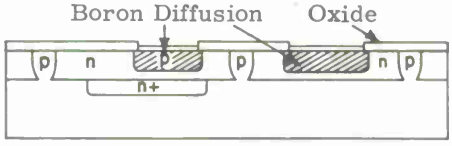
8. Isolation Diffusion: High-concentration predeposited p-type (boron) 10^{20} atoms/cc is diffused from surface through epitaxial layer to substrate, forming electrically isolated n regions.



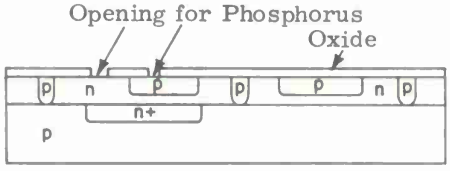
9. Base Mask: This step etches areas for base and resistor diffusion.



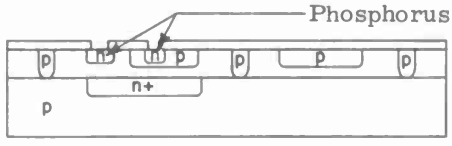
10. Boron Diffusion: This light-concentration diffusion is p-type BB_{r3} of 200 ohms/square sheet resistance. Sheet resistance is used instead of Co because of resistor value. Resistor and base mask are designed around 200 ohms/square diffusion. This is a difficult diffusion to control.



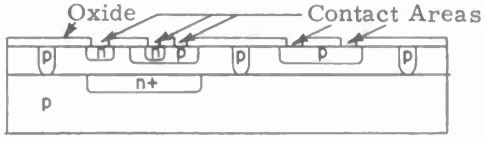
11. Emitter Mask: This mask will define areas for transistors, emitters, and collector diffusion.



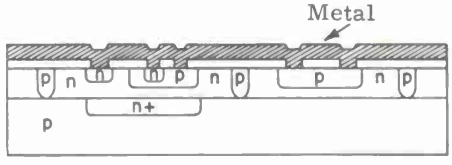
12. Phosphorus Diffusion: This is a high-concentration n-type diffusion. Its Co is in the order of 10^{21} and a micron in depth. High Co diffusion is essential in producing proper electrical parameters.



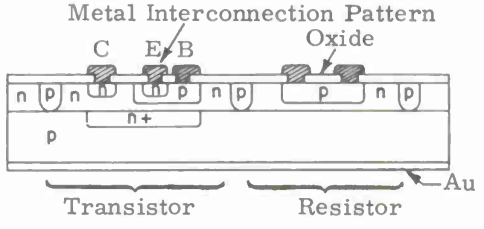
13. Contact Mask: Slice is photoresist processed for fifth time. Areas are etched away for ohmic contact.



14. Metallization: Entire slice is covered with thin metal film.



15. Metallization Mask: With one more series of photoresist process, the portion not needed for interconnections, contacts, and bonding areas is removed. Aluminum metallization is sintered at 570°C. Back side is etched and gold evaporated to insure good mounting.



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TEXT BOOKS ON PRESENT STATE OF THE ART

Burger, R.M. and R.P. Donovan, Fundamentals of Silicon Integrated Device Technology, Vol. l, Oxidation, Diffusion, and Epitaxy (Prentice-Hall, Englewood Cliffs, New Jersey, 1967).

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Warner, R.M., Jr., Editor, Integrated Circuits, Design Principles and Fabrication (McGraw-Hill, New York, 1965).

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13. ABSTRACT

This technical note describes the processing steps and technical considerations involved in fabricating bipolar integrated circuits. Basic processes and examples of the use of these to fabricate semiconductor devices are illustrated. A bibliography of basic references to the technology and a short list of current, useful textbooks on the present state of the art are also included.

14. KEY WORDS

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bonding

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